VIJAY PRATAP SHARMA

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OBJECTIVE

Ph.D. Scholar in Electrical Engineering at IIT Indore with approximately 6 years of combined research and industry experience in digital electronics, embedded systems, RTL design, ASIC/VLSI implementation, and AI hardware acceleration. Experienced in end-to-end hardware development spanning architectural exploration, RTL design, verification, synthesis, physical design, and GDSII implementation. Specialized in energy-efficient Edge-AI accelerators, trans-precision and low-bit computing, RISC-V processor architectures, hardware–software co-design, FPGA prototyping, and PPA optimization for DNN and TinyML workloads. Strong research and implementation experience in developing high-performance, area-efficient, and energy-conscious computing architectures.

EDUCATION

Doctor of Philosophy, Indian Institute of Technology Indore **2024 – Dec 2026**
Thesis: Algorithm–Precision Co-Design of Energy-Efficient Edge Intelligence Systems.

Master of Technology, Oriental University, Indore, India **2019 – 2022**
Thesis: Analysis and Implementation of MAC Unit for Different Precisions.

TECHNICAL SKILLS

HDL & RTL Design	Verilog, SystemVerilog
RTL Synthesis	Synopsys Design Vision, Fusion Compiler, Cadence Genus
Physical Design	Synopsys ICC-II, Cadence Innovus; CMOS 65 nm, 28 nm
Physical Verification	Siemens Calibre
Formal Verification & STA	Synopsys PrimeTime, Cadence Tempus, Cadence JasperGold, Cadence Conformal
Analog Design	Cadence Virtuoso
FPGA Implementation	AMD Vivado, Vivado HLS, VC707, PYNQ-Z2
Programming	C, Python
Scripting & Tools	Linux/Bash, LaTeX, Tcl, RISC-V GNU toolchain (Basic)

PROFESSIONAL EXPERIENCE

Senior Research Fellow **Apr 2025 – Present**
NSDCS Lab, IIT Indore | Indore, India
Project Supervisor: Prof. Santosh Kumar Vishvakarma

- Worked on hardware–software integration, FPGA deployment, peripheral interfacing, and system-level validation of the Falcon-XR platform.

Junior Research Fellow **Nov 2023 – Oct 2025**
NSDCS Lab, IIT Indore Indore, India

- Designed TREA (Time-Multiplexed Resource-Efficient Accelerator), a low-power and resource-efficient Edge-AI accelerator using time-multiplexed execution and low-bit quantization for efficient DNN inference.
- Contributed to the RTL-to-GDSII implementation, verification, synthesis, and physical design of an indigenous RISC-V processor for ASIC tapeout.

Design Engineer – Synthesis & Quality Check **Jun 2022 – Oct 2023**
Modernize Chip Solutions Pvt. Ltd. Bengaluru, India

- Worked in a semiconductor design environment with synthesis and design-quality activities; client location: MediaTek Bangalore Private Limited.
- Supported synthesis-related analysis and design quality checks for digital hardware.

Research Assistant **Jun 2021 – May 2022**
NSDCS Lab, IIT Indore Indore, India
Project Supervisor: Prof. Santosh Kumar Vishvakarma

- Designed and implemented a multi-precision Multiply–Accumulate (MAC) unit supporting different arithmetic precisions for efficient AI and DSP workloads, focusing on performance, power, and hardware optimization.
- Applied digital design fundamentals and computer architecture concepts to RTL-based hardware development.
- Developed RTL and hardware implementations using Verilog/SystemVerilog.

Electronics / Embedded Systems Engineer **Apr 2017 – May 2019**
Maxerience Electrosystems Private Limited Noida, India

- Developed and validated embedded electronic systems with emphasis on digital hardware, microcontroller-based control, and real-time data acquisition.
- Designed digital and analog hardware modules, including sensor interfaces, control circuits, peripheral interfaces, and electronic prototypes.
- Implemented embedded control algorithms using Embedded C and integrated microcontrollers with sensors and external hardware.
- Performed hardware debugging, functional testing, troubleshooting, and system-level validation of electronic prototypes.

RESEARCH PROJECTS

Visitor Research Intern **Apr 2025 – Present**
The University of Ljubljana Remote
Project Supervisor: Dr. Ratko Pilipović

- Contributed to concept formulation, RTL design, verification, and ASIC implementation of resource-efficient Edge-AI accelerators for object detection and classification.
- Developed ULTRA-MACE, a unified low-bit trans-precision reconfigurable MAC engine supporting FP4, FP8, Posit, and integer arithmetic for accelerated AI computing.
- Developed FALCON-XR, a flexible and hybrid low-precision floating-point compute engine for energy-efficient XR perception acceleration, targeting high-performance and resource-efficient processing of XR workloads.

Master's Thesis / Internship **Jul 2019 – Feb 2022**
Oriental University, Indore Indore, India
Project Supervisor: Dr. Hemant Patidar

- Designed and implemented multi-precision Multiply–Accumulate (MAC) architectures for AI and DSP applications.
- Designed and analyzed pipelined MAC architectures supporting different numerical precisions to improve performance, area, and power efficiency.
- Implemented and validated hardware designs using Verilog HDL on Xilinx FPGA platforms, including Spartan-3E, Spartan-6, and Virtex-5.
- Performed synthesis, timing analysis, and hardware validation using Xilinx ISE and ModelSim to evaluate resource utilization and operating frequency.

OTHER PROJECTS

- Traffic Light Control System: Developed a digital hardware model using LEDs and digital logic, demonstrating sequential circuit design and finite-state-machine (FSM) implementation.
- Cell Phone Detector: Designed and implemented an electronic system using analog/RF components to detect active mobile-phone signals in nearby areas.
- CMOS Adder Design: Designed and analyzed speed- and power-efficient CMOS adder architectures.

PUBLICATIONS

- **Vijay Pratap Sharma**, S. Venkatpurwar, M. Lokhande, R. Pilipović, and S. K. Vishvakarma, "ULTRA-MACE: A Unified Low-bit Trans-precision Reconfigurable Multiply-Accumulate Compute Engine for Accelerated Computing," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (IEEE TCAD)*, May 2026.
- **Vijay Pratap Sharma**, M. Lokhande, R. Pilipović, O. Kokane, and S. K. Vishvakarma, "TREA: Low-precision Time-Multiplexed, Resource-Efficient Edge Accelerator for Object Detection and Classification," *arXiv preprint*, arXiv:2605.07321, May 2026. [**Under Review]**
- **Vijay Pratap Sharma**, S. Venkatpurwar, S. Kumar, R. Pilipović, M. Lokhande, and S. K. Vishvakarma**,** "FALCON-XR: Flexible and Hybrid Low-Precision Floating-Point Compute Engine for Energy-Efficient XR Perception Acceleration," 2026**. [Under Review]**
- **Vijay Pratap Sharma,** S. V. Jayachand, Omkar Kokane, and Santosh Kumar Vishvakarma, "SPARV: A Small-footprint, Performance-accelerated RISC-V for TinyML Applications," *IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, Kolkata, India, Jul. 7–10, 2026.
- Additional contributions: Google Scholar.

REFERENCES

Dr. Santosh Kumar Vishvakarma | Professor, Department of Electrical Engineering, IIT Indore
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Dr. Vaibhav Neema | Professor, Institute of Engineering and Technology, Devi Ahilya University, Indore
Email: vneema@ietdavv.edu.in | **Contact:** +91 9174738874

Dr. Ratko Pilipović | Assistant Professor, Faculty of Computer and Information Science, University of Ljubljana, Slovenia
Email: ratko.pilipovic@fri.uni-lj.si